WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device incorporating a semiconductor memory circuit and a control circuit for controlling a data access to the semiconductor memory circuit,

wherein the control circuit outputs an address signal of several bits in which only a value of 1 bit changes in a sequential order when a data access by consecutive addresses is performed on the semiconductor memory circuit.

2. The semiconductor integrated circuit device according to claim 1, wherein the semiconductor memory circuit includes at least one selected from a ROM circuit and a RAM circuit.

3. A semiconductor integrated circuit device incorporating a semiconductor memory circuit and a control circuit for controlling a data access to the semiconductor memory circuit,

wherein the control circuit includes an address generation circuit, and the address generation circuit outputs an address signal of several bits in which only a value of 1 bit changes in a sequential order when a data access by consecutive addresses is performed on the semiconductor memory circuit.

4. The semiconductor integrated circuit device according to claim 3, wherein the semiconductor memory circuit includes at least one selected from a ROM circuit and a RAM circuit.

5. The semiconductor integrated circuit device according to claim 3, further comprising means for converting a location of data stored in the semiconductor memory circuit into a location corresponding to a change in the address signal from the address generation circuit.

6. A semiconductor integrated circuit device incorporating a semiconductor memory circuit and a control circuit for controlling a data access to the semiconductor memory circuit,

wherein the control circuit includes an address generation circuit that divides a clock to be input, performs a phase adjustment by sampling the divided clock and generates an address signal of several bits, and the address generation circuit outputs the address signal of several bits in which only a

value of 1 bit changes in a sequential order when a data access by consecutive addresses is performed on the semiconductor memory circuit.

7. The semiconductor integrated circuit device according to claim 6, wherein the semiconductor memory circuit includes at least one selected from a ROM circuit and a RAM circuit.

8. The semiconductor integrated circuit device according to claim 6, further comprising means for converting a location of data stored in the semiconductor memory circuit into a location corresponding to a change in the address signal from the address generation circuit.

9. A semiconductor integrated circuit device incorporating a semiconductor memory circuit and a control circuit for controlling a data access to the semiconductor memory circuit,

wherein the control circuit includes an address generation circuit that divides a clock to be input and generates an address signal of several (m) bits in which bit 0 is set as a lowest-order bit, and the address generation circuit outputs the address signal of several bits in which only a value of 1 bit changes in a sequential order by dividing the clock by $(1/4) \times (1/2)^i$ to generate bit i (i = 0 to (m-1)) and delaying a phase of each bit by 1/4 cycle with respect to a cycle of an immediately lower-order bit when a data access by consecutive addresses is performed on the semiconductor memory circuit.

10. The semiconductor integrated circuit device according to claim 9, wherein the semiconductor memory circuit includes at least one selected from a ROM circuit and a RAM circuit.

11. The semiconductor integrated circuit device according to claim 9, further comprising means for converting a location of data stored in the semiconductor memory circuit into a location corresponding to a change in the address signal from the address generation circuit.

12. A semiconductor integrated circuit device incorporating a timer counter circuit, the timer counter circuit comprising:

a counter circuit that divides a clock to be input by a predetermined division rate and outputs a plurality of divided clocks,

a counter register that stores a divided clock corresponding to an immediately higher-order bit as data based on a divided clock corresponding to a low-order bit to be output from the counter circuit and outputs a count value in which only a value of 1 bit changes in a sequential order,

a compare register that stores a predetermined comparison set value, and

a compare circuit that compares the count value from the counter register with the predetermined comparison set value from the compare register and outputs a comparison result thereof.

13. The semiconductor integrated circuit device according to claim 12, further comprising means for converting the comparison set value stored in the compare register into a value corresponding to a change in the count value from the counter register.